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Mani Adeli

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application for:

Steven Teig, et al.

Serial No.: 09/731,891

Filing Date: 12/06/2000

For: METHOD AND APPARATUS FOR CONSIDERING DIAGONAL WIRING IN PLACEMENT

Examiner: Thuan V. Do

Group Art Unit: 2825

APPEAL BRIEF

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is an Appeal from the final rejection of claims 4-13, 43-64, and 88-96 in the above-referenced application. In accordance with 37 C.F.R. § 41.37, this Appeal Brief, along with the accompanying Appendix, is accompanied by the required fee. Please charge any additional fees or credit any overpayment to Deposit Account No. **50-1128**.

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Client Docket: 2002-077 Y1
Attorney Docket: SPLX.P0002
PTO Serial Number 09/731,891

I. REAL PARTY IN INTEREST

The real party in interest to this Appeal is Cadence Design Systems, a Delaware Corporation, having its principal place of business in San Jose, California.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellants, the Appellants' legal representative, or assignees thereof.

III. STATUS OF CLAIMS

Claims 1-3, 14-42 and 65-87 are canceled in the present application. Claims 4-10, 12-13, 43-45, 48-49, 51-64, and 88-96 are pending in the present application. The Examiner has rejected claims 4-10, 12-13, 43-45, 48-49, 51-64, and 88-96. Furthermore, the Examiner objected to claims 11, 46-47 and 50 as being dependent upon a rejected base claim. Appellants hereby appeals the rejection of claims 4-10, 12-13, 43-45, 48-49, 51-64, and 88-96.

IV. STATUS OF AMENDMENTS

No amendments to the application were submitted after final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A. Independent Claim 4

Claim 4 recites a method for placing circuit modules in an integrated circuit ("IC") layout,

The IC layout has a number of circuit elements and a net. The net has a set of circuit elements. *Specification, page 20, line 16 to page 21, line 7.* The method uses a diagonal line to measure a placement metric. *See specification, page 14, lines 8-9.* The method of using the diagonal line to measure the placement metric includes calculating an estimate of the length of interconnect lines necessary to connect the circuit elements of the net during a routing operation. The calculation measures the length of at least one line that is at least partially diagonal. *Specification, page 18, lines 3-16; see also, Figures 9* and *11.*

B. Independent Claim 43

Claim 43 recites a method of placing circuit modules in an integrated circuit ("IC") layout, where the IC layout includes a net having several circuit elements. *Specification, page 20, line 16 to page 21, line 7.* The method constructs a connection graph that connects the circuit elements of the net. The connection graph has edges, where at least one of the edges is at least partially diagonal. *See Figures 11 and 13.* The method identifies a placement metric based on the connection graph. *Specification, page 29, lines 10-13; see also specification, page 35, lines 1-4.* The method uses the connection graph to identify a placement of the circuit modules. *Specification, page 29, lines 14-16; see also specification 35, lines 5-7.*

C. Independent Claim 58

For an electronic design automation ("EDA") application, claim 58 recites a method of placing circuit modules in an integrated circuit ("IC") layout. The IC layout includes several nets,

each of which includes several circuit elements in the IC layout. *Specification, page 2, lines 5-10.* The EDA application includes a wiring model that defines different types of interconnect lines. The interconnect lines are for connecting the circuit elements of the nets. The wiring model has diagonal lines. *Specification, page 16, lines 1-5; see also Figure 7.* For each particular net, the method defines a minimum spanning tree that models the topology of interconnect lines for connecting the circuit elements of the particular net. *Specification, page 25, lines 5-16.* The minimum spanning tree has edges, where at least one of the edges of at least one of the minimum spanning trees is at least partially diagonal. *Specification, page 25, line 18.* The method calculates the length of the edges of the minimum spanning trees. The method combines the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets during a routing operation. *See Figure 12; see also specification, page 28, lines 6-10.* The method uses the combined length calculations to identify a placement of the circuit modules. *Specification, page 29, lines 14-16.*

D. Independent Claim 61

For an electronic design automation ("EDA") application, claim 61 recites a method of placing circuit modules in an integrated circuit ("IC") layout. The IC layout includes several nets, each of which includes several circuit elements in the IC layout. *Specification, page 2, lines 5-10.* The EDA application includes a wiring model that defines different types of interconnect lines. The interconnect lines are for connecting the circuit elements of the nets. The wiring model has diagonal lines. *Specification, page 16, lines 1-5; see also Figure 7.* The method, for each particular net,

defines a Steiner tree that models the topology of interconnect lines for connecting the circuit elements of the particular net. *See Figure 13.* The Steiner tree has edges, where at least one of the edges of at least one of the Steiner trees is at least partially diagonal. *Specification, page 30, line 10.* The method calculates the length of the Steiner trees. *See Figure 14; see also specification, page 32, lines 16-19.* The method combines the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets during a routing operation. *Specification, page 35, lines 1-4.* The method uses the combined length calculations to identify a placement of the circuit modules. *Specification 35, lines 5-7*

E. Independent Claim 88

Claim 88 recites a method of placing circuit modules in an integrated circuit ("IC") layout. The IC layout includes a set of circuit elements. *Specification, page 20, line 16 to page 21, line 7.* The method identifies a connection graph that connects the set of circuit elements, where (1) the connection graph has several edges, and (2) at least two of the edges are neither parallel nor orthogonal to each other. *See Figures 11 and 13.* The method identifies a placement metric based on the connection graph. *Specification, page 29, lines 10-13; see also specification, page 35, lines 1-4.* The method uses the connection graph to identify a placement of the circuit modules. *Specification, page 29, lines 14-16; see also specification 35, lines 5-7.*

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Whether the appealed claims are unpatentable under 35 U.S.C. § 112, second paragraph, as particularly pointing out and distinctly claiming the subject matter which the Appellants regard as the invention.

II. Whether the appealed claims are unpatentable under 35 U.S.C. § 102(e) over United States Patent 6,301,686, issued to Kikuchi ("Kikuchi").

VII. ARGUMENT

The Examiner erred in rejecting the claimed invention by misapplying standards under 35 U.S.C. § 112, second paragraph and 35 U.S.C. § 102(e).

A. The Appealed Claims Are Patentable Under 35 U.S.C. § 112, Second Paragraph.

In rejecting the subject claims under 35 U.S.C. § 112, second paragraph, the Examiner stated the following:

> The term "during a routing operation" is unclear [as] to what it means by [the] specification. *Office Action mailed October 21, 2004, page 2.*

Appellants' use of the term "during a routing operation" is clear. The test for definiteness under 35 U.S.C. 112, second paragraph, is whether "those skilled in the art would understand what is claimed when the claim is read in light of the specification." *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576, 1 USPQ2d 1081, 1088 (Fed. Cir. 1986). *See* MPEP 2173.02.

Appellants respectfully submit that those skilled in the art would understand what is claimed when the term "during a routing operation" is read in light of the specification. A routing operation is an operation that is performed during an IC design process. *Specification, page 3, line 11.* During a routing operation, a router defines interconnect lines between circuits modules that were placed during a placement operation. *See Specification, page 3, lines 10-11.* As such, the term "during a routing operation" means during an operation that defines interconnect lines between circuit modules/elements. *Specification, page 3, line 11.* Therefore, the term "during a routing operation" is definite under 35 U.S.C. § 112, second paragraph.

B. The Appealed Claims Are Patentable Under 35 U.S.C. § 102(e) Over Kikuchi.

In rejecting the subject claims under 35 U.S.C. § 102(e), the Examiner stated the following:

> Kikuchi teaches calculat[ing] a direction connecting from the component terminal A to the component terminal B to obtain a distance between the component terminal A and the component terminal B as a length of the third graph for determining 2 lines (two components of the same net are formulated by an angled node and 2 terminals A and B) of an angle that meets the limitation of the claim. That calculation is performed in routing process as indicated at least in [F]igure 5, boxes s411, s412 for matching the new adding area of "during a routing operation" and the lengths in formulated angles (capacity area) including diagonal lines obviously are taught in col. 11, lines 1-18. In consequence, Kikuchi determines the length of partial diagonal line represented by combination of calculated terminal A and B and a node after the length calculation of the third graph. *Office Action mailed October 21, 2004, pages 4-5.*

1. Kikuchi Does not Disclose, Teach or Suggest Each and Every Element of the Claims.

Appellants respectfully submit that Kikuchi does not disclose, teach or suggest each and

every element of the claims. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

a. Kikuchi Describes a Graph Generator for Calculating a Minimum Distance Between Two Components Based on The Bandwidth Between the Two Components.

Kikuchi describes a method for compacting an integrated circuit ("IC") layout, where (1) the IC layout includes components and routes, and (2) the compaction can be performed in both the longitudinal and lateral directions at once. *Kikuchi, column 4, lines 9-12.* The compaction method calculates a movement area limit for a first component within which the first component can move in any direction towards a second component in consideration of a route bandwidth. *See Kikuchi, column 4, lines 18-22.*

The route bandwidth is the number of routes that pass through the first and second components. *See Kikuchi, column 4, lines 22-24.* These routes do not connect the first and second components. *See Kikuchi, Figures 8A and 8B.* The movement area limit (e.g., the length between the first and second components) is based on the necessary total widths of the routes that pass through the first and second components. In other words, the movement area limit (e.g., length) is based on the *route congestion* between the first and second components. The Examiner is applying the length

of the movement area limit to mean the length of the interconnect lines necessary to connect the circuit elements. However, as shown in **Figures 8A** and **8B**, the movement area limit (e.g., length) is not based on an estimate of the length of interconnect lines necessary to connect the circuit elements of the net during a routing operation. Thus, the Examiner is incorrectly applying a length associated with a congestion attribute between the first and second components to mean a length associated with the interconnect lines necessary to connect the circuits elements during a routing operation.

Furthermore, the length associated with the movement area limit is not a connection graph that connects the circuit elements of the net. A net is a collection of pins that need to be electrically connected with interconnect lines. *Specification, page 2, lines 15-18.* The pins illustrate circuit modules and are geometric representations of circuit components. *Specification, page 2, lines 11-13.* As such, a connection graph that connects the circuits elements of the net, represents a graph of the interconnect lines of the circuit elements.

As mentioned above, Kikuchi does not describe an estimate length associated with the interconnect lines necessary to connect the circuits elements. Therefore, by virtue of the fact that a net includes interconnect lines necessary to connect the circuit elements, Kikuchi does not describes a connection graph that connects the circuit elements of the net.

b. Kikuchi's Figure 5 Illustrates a Method for Generating a Terminal Graph That Calculates a Graph Based on Congestion.

The Examiner cites **Figure 5** of Kikuchi as disclosing the claimed invention. However, **Figure 5** illustrates a method for generating a terminal graph that calculates a graph based on

congestion. Kikuchi describes a method that connects a graph between first and second components. *Kikuchi, column 10, lines 58-60*. Kikuchi's method moves the first and second components from an upper end of the substrate towards a lower end of the substrate. *See Kikuchi, column 10, lines 50-51*.

These first and second components are moved until the length of the graph that connects the first and second components is shorter than the length of the graph for the first and second components at a previous location. *Kikuchi, column 11, lines 19-20*. The movement of the first and second components is based on a constraint graph prepared during step **s101** and **s102**. *See Kikuchi, Figure 4*. During these steps (e.g., **s101 and s102**), the method (1) prepares segment data based on the initial IC layout, (2) calculates a movement area limit for the components, and (3) prepares a constraint graph based on the segment data and movement area limit. *Kikuchi, column 8, lines 45-55; see also column 7, lines 57-61; see also column 9, line 65 to column 10, line 23*.

As mentioned above, the movement area limit for a particular component is based on the number of routes that pass through that particular component and another component. *See Kikuchi, column 7, lines 62-65*. Therefore, the graph (e.g., terminal graph) described by Kikuchi is not based on an estimate of the length of interconnect lines necessary to connect the circuit elements of the net during a routing operation. As shown in **Figures 8A** and **8B**, the terminal graph does not represent interconnect lines between circuit elements. Therefore, the length of the terminal graph does not represent the length of interconnect lines necessary to connect the circuit elements of the net during a routing operation.

As further shown in both **Figures 8A** and **8B**, the routes (e.g., interconnect lines) are distinct from the terminal graph, which indicates that the terminal graph is not a route (e.g., interconnect line). Thus, the Examiner is incorrectly applying a length associated with a terminal graph (which is based on a routing bandwidth) between the first and second components to mean a length associated with the interconnect lines necessary to connect the circuits elements during a routing operation.

Furthermore, Kikuchi's terminal graph is not a connection graph that connects the circuit elements of the net. As mentioned above, a net is a collection of pins that need to be electrically connected with interconnect lines. *Specification, page 2, lines 15-18.* The pins illustrate circuit modules and are geometric representations of circuit components. *Specification, page 2, lines 11-13.* As such, a connection graph that connects the circuits elements of the net, represents a graph of the interconnect lines of the circuit elements.

As mentioned above, Kikuchi's terminal graph terminal graph does not represent the length of interconnect lines necessary to connect the circuit elements of the net. Therefore, by virtue of the fact that a net includes interconnect lines necessary to connect the circuit elements, Kikuchi's terminal graph is not a connection graph that connects the circuit elements of the net.

2. Each and Every Element of the Claims Are Not Anticipated by Kikuchi.

a. Independent Claim 4

Claim 4 recites a method for placing circuit modules in an integrated circuit ("IC") layout, The IC layout has a number of circuit elements and a net. The net has a set of circuit elements.

Specification, page 20, line 16 to page 21, line 7. The method uses a diagonal line to measure a placement metric. *See specification, page 14, lines 8-9.* The method of using the diagonal line to measure the placement metric includes calculating an estimate of the length of interconnect lines necessary to connect the circuit elements of the net during a routing operation. The calculation measures the length of at least one line that is at least partially diagonal. *Specification, page 18, lines 3-16; see also, Figures 9* and *11.*

Kikuchi does not disclose, teach or suggest each and every element of claim 4. For example, Kikuchi does not describe the method for using the diagonal line to measure the placement metric that includes calculating an estimate of the length of interconnect lines necessary to connect the circuit elements of the net during a routing operation, as recited in claim 4. Instead, as mentioned above, Kikuchi describes a terminal graph for determining congestion between two components. *See Kikuchi, column 7, lines 62-65.* The length of this terminal graph is not an estimate of the length of interconnect lines necessary to connect the circuit elements of the net during a routing operation.

b. Independent Claim 43

Claim 43 recites a method of placing circuit modules in an integrated circuit ("IC") layout, where the IC layout includes a net having several circuit elements. *Specification, page 20, line 16 to page 21, line 7.* The method constructs a connection graph that connects the circuit elements of the net. The connection graph has edges, where at least one of the edges is at least partially diagonal. *See Figures 11 and 13.* The method identifies a placement metric based on the connection graph.

Specification, page 29, lines 10-13; see also specification, page 35, lines 1-4. The method uses the connection graph to identify a placement of the circuit modules. *Specification, page 29, lines 14-16; see also specification 35, lines 5-7.*

Kikuchi does not disclose, teach or suggest each and every element of claim 43. For example, Kikuchi does not describe a method for constructing a connection graph that connects the circuit elements of the net, as recited in claim 43. Instead, as mentioned above, Kikuchi describes a terminal graph for determining congestion between two components. *See Kikuchi, column 7, lines 62-65.* The length of this terminal graph is not a connection graph that connects the circuit elements of the net.

c. Independent Claim 58

For an electronic design automation ("EDA") application, claim 58 recites a method of placing circuit modules in an integrated circuit ("IC") layout. The IC layout includes several nets, each of which includes several circuit elements in the IC layout. *Specification, page 2, lines 5-10.* The EDA application includes a wiring model that defines different types of interconnect lines. The interconnect lines are for connecting the circuit elements of the nets. The wiring model has diagonal lines. *Specification, page 16, lines 1-5; see also Figure 7.* For each particular net, the method defines a minimum spanning tree that models the topology of interconnect lines for connecting the circuit elements of the particular net. *Specification, page 25, lines 5-16.* The minimum spanning tree has edges, where at least one of the edges of at least one of the minimum spanning trees is at least partially diagonal. *Specification, page 25, line 18.* The method calculates the length of the edges of

the minimum spanning trees. The method combines the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets during a routing operation. *See Figure 12; see also specification, page 28, lines 6-10.* The method uses the combined length calculations to identify a placement of the circuit modules. *Specification, page 29, lines 14-16.*

Kikuchi does not disclose, teach or suggest each and every element of claim 58. For example, Kikuchi does not describe a method for combining the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets during a routing operation, as recited in claim 58. Instead, as mentioned above, Kikuchi describes a terminal graph for determining congestion between two components. *See Kikuchi, column 7, lines 62-65.* The length of this terminal graph is not a minimum spanning tree that models the topology of interconnect lines for connecting the circuit elements of the particular net.

d. Independent Claim 61

For an electronic design automation ("EDA") application, claim 61 recites a method of placing circuit modules in an integrated circuit ("IC") layout. The IC layout includes several nets, each of which includes several circuit elements in the IC layout. *Specification, page 2, lines 5-10.* The EDA application includes a wiring model that defines different types of interconnect lines. The interconnect lines are for connecting the circuit elements of the nets. The wiring model has diagonal lines. *Specification, page 16, lines 1-5; see also Figure 7.* The method, for each particular net,

defines a Steiner tree that models the topology of interconnect lines for connecting the circuit elements of the particular net. *See Figure 13.* The Steiner tree has edges, where at least one of the edges of at least one of the Steiner trees is at least partially diagonal. *Specification, page 30, line 10.* The method calculates the length of the Steiner trees. *See Figure 14; see also specification, page 32, lines 16-19.* The method combines the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets during a routing operation. *Specification, page 35, lines 1-4.* The method uses the combined length calculations to identify a placement of the circuit modules. *Specification 35, lines 5-7*

Kikuchi does not disclose, teach or suggest each and every element of claim 61. For example, Kikuchi does not describe a method for combining the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets during a routing operation, as recited in claim 61. Instead, as mentioned above, Kikuchi describes a terminal graph for determining congestion between two components. *See Kikuchi, column 7, lines 62-65.* The length of this terminal graph is not a Steiner tree that models the topology of interconnect lines for connecting the circuit elements of the particular net.

e. Independent Claim 88

Claim 88 recites a method of placing circuit modules in an integrated circuit ("IC") layout. The IC layout includes a set of circuit elements. *Specification, page 20, line 16 to page 21, line 7.* The method identifies a connection graph that connects the set of circuit elements, where (1) the

connection graph has several edges, and (2) at least two of the edges are neither parallel nor orthogonal to each other. *See Figures 11 and 13*. The method identifies a placement metric based on the connection graph. *Specification, page 29, lines 10-13; see also specification, page 35, lines 1-4.* The method uses the connection graph to identify a placement of the circuit modules. *Specification, page 29, lines 14-16; see also specification 35, lines 5-7.*

Kikuchi does not disclose, teach or suggest each and every element of claim 88. For example, Kikuchi does not describe a method for identifying a connection graph that connects the set of circuit elements, as recited in claim 88. Instead, as mentioned above, Kikuchi describes a terminal graph for determining congestion between two components. *See Kikuchi, column 7, lines 62-65*. The length of this terminal graph is not a connection graph that connects the set of circuit elements.

VIII. CLAIMS APPENDIX

See Appendix A attached.

IX. EVIDENCE APPENDIX

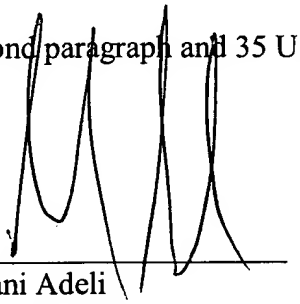
In this Appeal Brief, Appellants have not provided an Evidence Appendix.

X. RELATED PROCEEDINGS APPENDIX

There are no related appeals or interferences known to the Appellants, the Appellants' legal representative, or assignees thereof. Therefore, in this Appeal Brief, Appellants have not identified related appeals and interferences.

XI. CONCLUSION

In view of the foregoing, Appellants respectfully submit that the claims are patentable. Appellants hereby request that the Board overturn the Examiner's finding that the claims are unpatentable under 35 U.S.C. § 112, second paragraph and 35 U.S.C. § 102(e).



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APPENDIX A

The following claims are the subject of this Appeal.

4. For an electronic design automation application, a method of placing circuit modules in an integrated circuit ("IC") layout, wherein the IC layout has a number of circuit elements, a net having a set of circuit elements, the method comprising:

using a diagonal line to measure a placement metric;

wherein using the diagonal line to measure a placement metric comprises calculating an estimate of the length of interconnect lines necessary to connect the circuit elements of said net during a routing operation, wherein the calculation measures the length of at least one line that is at least partially diagonal.

5. The method of claim 4, wherein calculating the estimate comprises constructing a bounding box encompassing all the circuit elements of the net.

6. The method of claim 5, wherein calculating the estimate further comprises using the diagonal line to measure an attribute of the bounding box.

7. The method of claim 6, wherein said attribute is the distance between two opposing corners of the bounding box, and said diagonal line traversing at least a portion of said distance.

8. The method of claim 6, wherein the diagonal line is 45° line.

9. The method of claim 4, wherein calculating the estimate comprises constructing a connection graph that models the topology of interconnect lines for connecting the circuit elements of the net, said connection graph having edges, wherein at least one of the edges is at least partially diagonal.

10. The method of claim 9, wherein calculating the estimate further comprises calculating the length of the edges of the graphs.

12. The method of claim 9, wherein the connection graph is a minimum spanning tree that includes a diagonal line and at least one of a horizontal line and a vertical line.

13. The method of claim 9, wherein the connection graph is a Steiner tree that includes a diagonal line and at least one of a horizontal line and a vertical line.

43. A method of placing circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a net having a plurality of circuit elements, the method comprising:

a) constructing a connection graph that connects the circuit elements of the net, said connection graph having edges, wherein at least one of the edges is at least partially diagonal;

b) identifying a placement metric based on the connection graph; and

c) using the connection graph to identify a placement of the circuit modules.

44. The method of claim 43 further comprising:

calculating the length of the edges of the graph; and

combining the length calculations of the edges of the graph.

45. The method of claim 44, wherein the combining of said length calculations comprises adding said measurements.

48. The method of claim 44, wherein the combined length calculation provides an estimate of interconnect-line length needed to connect the circuit elements of the net.

49. The method of claim 48, wherein said estimate is measured to obtain a placement cost of an initial placement configuration.

51. The method of claim 44, wherein the IC layout includes a plurality of nets, each net having a plurality of circuit elements, the method comprising:

a) for each particular net, constructing a connection graph that connects the circuit elements of the particular net, said connection graphs having edges, wherein some of the edges are at least partially diagonal;

b) calculating the length of the edges of the graphs; and

c) combining the length calculations to obtain an estimate of the interconnect-line length needed for connecting the circuit elements of the nets.

52. The method of claim 43, wherein the diagonal edge forms a 45° angle with respect to

a side of the IC layout.

53. The method of clam 43, wherein the diagonal edge forms a 120° angle with respect to a side of the IC layout.

54. The method of claim 43, wherein the circuit elements include pins of circuit modules.

55. The method of claim 43, wherein the circuit elements include circuit modules.

56. The method of claim 43, wherein the connection graph is a minimum spanning tree.

57. The method of claim 43, wherein the connection graph is a Steiner tree.

58. For an electronic design automation application, a method of placing circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a plurality of nets each of which includes a plurality of circuit elements in the IC layout, wherein the EDA application includes a wiring model that defines different types of interconnect lines for connecting the circuit elements of the nets, said wiring model having diagonal lines, the method comprising:

a) for each particular net, defining a minimum spanning tree that models the topology of interconnect lines for connecting the circuit elements of the particular net, said minimum spanning tree having edges, wherein at least one of the edges of at least one of the minimum spanning trees is at least partially diagonal;

b) calculating the length of the edges of the minimum spanning trees;

c) combining the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets during a routing operation; and

d) using the combined length calculations to identify a placement of the circuit modules.

59. The method of claim 58, wherein some of the diagonal edges are in the same direction as some of the diagonal lines in the wiring model.

60. The method of claim 58 further comprising:

a) moving a circuit element from a first location in the IC layout to a second location in this layout;

b) for each net containing the moved circuit element, defining a new minimum spanning tree that models the topology of interconnect lines for connecting the circuit elements of the particular net after the move, said minimum spanning trees having edges, wherein at least one of the edges of at least one of the minimum spanning trees is at least partially diagonal; and

c) calculating the length of the new minimum spanning trees to estimate the change in the total interconnect-line length.

61. For an electronic design automation application, a method of placing circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a plurality of nets each of

which includes a plurality of circuit elements in the IC layout, wherein the EDA application includes a wiring model that defines different types of interconnect lines for connecting the circuit elements of the nets, said wiring model having diagonal lines, the method comprising:

a) for each particular net, defining a Steiner tree that models the topology of interconnect lines for connecting the circuit elements of the particular net, said Steiner tree having edges, wherein at least one of the edges of at least one of the Steiner trees is at least partially diagonal;

b) calculating the length of the Steiner trees;

c) combining the length calculations to obtain an estimate of the total interconnect-line length needed for connecting the circuit elements of the nets during a routing operation; and

d) using the combined length calculations to identify a placement of the circuit modules.

62. The method of claim 61, wherein some of the diagonal edges are in the same direction as some of the diagonal lines in the wiring model.

63. The method of claim 61 further comprising defining a set of Steiner points for at least some of the nets.

64. The method of claim 61 further comprising:

a) moving a circuit element from a first location in the IC layout to a second location in this layout;

b) for each net containing the moved circuit element, defining a new Steiner tree that models the topology of interconnect lines for connecting the circuit elements of the particular net after the move, said new Steiner trees having edges, wherein at least one of the edges of at least one of the new Steiner trees is at least partially diagonal; and

c) calculating the length of the new Steiner trees to estimate the change in the total interconnect-line length.

88. A method of placing circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a set of circuit elements, the method comprising:

a) identifying a connection graph that connects the set of circuit elements, wherein said connection graph has a plurality of edges, wherein at least two of the edges are neither parallel nor orthogonal to each other;

b) identifying a placement metric based on the connection graph; and

c) using the connection graph to identify a placement of the circuit modules.

89. The method of claim 88, wherein identifying a placement metric comprises calculating the length of the graph.

90. The method of claim 89, wherein the length provides an estimate of interconnect-line length needed to connect the circuit elements of the net.

91. The method of claim 90, wherein said placement metric estimate is identified to obtain a placement cost of an initial placement configuration.

92. The method of claim 90, wherein said placement metric estimate is identified to obtain a placement cost of a modified placement configuration.

93. The method of clam 88, wherein the edges that are neither parallel nor orthogonal forms a 45° angle with respect to each other.

94. The method of clam 88, wherein the edges that are neither parallel nor orthogonal forms a 120° angle with respect to each other.

95. The method of claim 88, wherein the connection graph is a minimum spanning tree.

96. The method of claim 88, wherein the connection graph is a Steiner tree.